What is claimed is:

1. A semiconductor memory device, comprising:

an oscillator circuit for generating an oscillation signal that varies based on a mode of operation;

a word line enable circuit for generating a word line enable signal in response to the oscillation signal; and

a control circuit for controlling the oscillator circuit and the word line enable circuit so that a pulse width of the word line enable signal is widened as operation mode of the memory device changes from an active mode to a stand-by mode.

2. The device of claim 1, wherein a period of the oscillation signal is maintained as operation mode changes due to the widening of the pulse width.

3. The device of claim 1, wherein the control circuit controls the oscillator circuit so that the period of the oscillation signal is lengthened after a given time elapses from the beginning of the stand-by mode.

4. The device of claim 3, the device including an array of memory cells arranged in row and columns, wherein all of the memory cells are refreshed for the given time to restore data therein.

5. The device of claim 1, wherein the period of the oscillation signal is equal to a refresh period.

6. The device of claim 5, wherein the control circuit controls the refresh period and the pulse width of the word line enable signal in response to a chip select signal.

7. The device of claim 3, wherein the pulse width of the word line enable signal is maintained equally during a refresh section of the stand-by mode.

8. A semiconductor memory device including an array of memory cells arranged in row and columns, comprising:

a flag signal generator circuit for generating a flag signal indicating an end of a first refresh section of a stand-by mode of operation, after a given time elapses from a start of the stand-by mode;

an oscillator circuit for generating a variable oscillation signal in response to the flag signal;

a word line enable circuit generating a word line enable signal in response to the oscillation signal; and

a row decoder circuit for selecting rows in response to row addresses and driving the selected rows during an activation period of the word line enable signal.

9. The device of claim 8, wherein the pulse width of the word line enable signal varies based on mode of operation of the device.

10. The device of claim 9, wherein

the stand-by mode of operation spans a period of time that includes the first refresh section and a second refresh section, and

the oscillation signal generated in the first refresh section has a longer period than the oscillation signal generated in the second refresh section.

11. The device of claim 8, wherein the flag signal generator circuit activates the flag signal after a given time elapses from an inactivation of a chip select signal.

12. The device of claim 11, wherein a pulse width of the word line enable circuit is varied according to the chip select signal.

13. The device of claim 8, wherein a word line enable signal that is generated during the first refresh section has a wider pulse width than a word line enable signal generated when the device is in an active mode of operation.

14. The device of claim 8, wherein the period of the oscillation signal in the first refresh section is equal to the period of the oscillation signal when the device is in an active mode of operation.

15. The device of claim 10, wherein the pulse width of the word line enable signal in the first refresh section is equal to the pulse width of the word line enable signal in the second refresh section.

16. The device of claim 8, wherein the flag signal generator circuit includes a counter operating in synchronization with the oscillation signal.

17. The device of claim 8, wherein the memory device is a pseudo static random access memory (PSRAM) having dynamic random access memory (DRAM) cells as the memory cells.

18. A semiconductor memory device including an array of memory cells arranged in row and columns, comprising:

a detector circuit activating a flag signal as a result of a detection of a given time that has elapsed from a beginning of a stand-by mode of operation of the device;

an oscillator circuit for generating an oscillation signal based on the flag signal;

a word line enable circuit for generating a word line enable signal that is synchronized with the oscillation signal; and

a row decoder circuit for selecting rows in response to row addresses and driving the selected rows during an active period of the word line enable signal.

19. The device of claim 18, wherein the oscillation signal has a first period during an inactive period of the flag signal and a second period during an active period of the flag signal.

20. The device of claim 19, wherein the second period is longer than the first period.

21. The device of claim 18, wherein a pulse width of the word line enable signal is widened at the beginning of the stand-by mode.

22. The device of claim 18, wherein the detector circuit includes a counter operating in synchronization with the oscillation signal.

23. The device of claim 18, wherein the memory cells are refreshed one time for the given time.

24. The device of claim 19, wherein the inactive period of the flag signal includes an active mode of operation and a first refresh section of the stand-by mode of operation, and the active period of the flag signal includes a second refresh section of the stand-by mode.

25. The device of claim 18, wherein the memory device includes a pseudo static random access memory (PSRAM) having dynamic random access memory (DRAM) cells as the memory cells.

26. A method of operating a semiconductor memory device having an active mode of operation and a stand-by mode of operation, comprising:

generating a flag signal indicating an end of a first refresh section of the stand-by mode;

generating an oscillation signal in response to the flag signal; and

generating a word line enable signal in response to the oscillation signal, the word line enable signal having a pulse width that varies depending on the mode of operation of the device.

27. The method of claim 26, wherein

the flag signal has an inactive period and an active period,

the inactive period of the flag signal includes the active mode and the first refresh section of the stand-by mode, and the active period of the flag signal includes a second refresh section of the stand-by mode of operation.

28. The method of claim 27, wherein

the oscillation signal is generated during the first refresh section and during the second refresh section of the stand-by mode, and

the oscillation signal generated in the first refresh section has a longer period than the oscillation signal generated during the second refresh section.

29. The method of claim 26, wherein the word line enable signal generated during the first refresh section of the stand-by mode has a wider pulse width than the word line enable signal generated during the active mode.

30. A control circuit for a semiconductor memory device, the device having an oscillation circuit for generating an oscillation signal and a word line enable circuit for generating a word line enable signal in response to the oscillation signal, the control circuit comprising:

a buffer circuit; and

a detector circuit,

wherein

the buffer circuit outputs a chip select signal to the detector circuit and the word line enable circuit, and

the detector circuit generates a flag signal for controlling the oscillation circuit based on a detection of a change in operation mode of the device.

31. The control circuit of claim 30, wherein the oscillation signal varies based on mode of operation of the device.

32. The control circuit of claim 30, wherein the buffer circuit and detector circuit control the oscillating circuit so that a period of the oscillation signal is maintained for a given period of time as the device changes mode of operation.

33. The control circuit of claim 30, wherein the buffer circuit and detector circuit control the word line enable circuit so that a pulse width of the word line enable signal is widened as the device changes from an active mode of operation to a stand-by mode of operation.

34. The control circuit of claim 30, wherein

the device has an active mode of operation and a standby-mode of operation, and

the stand-by mode of operation spans a duration that includes at least two periods of time, represented as a first refresh section and a section refresh section.

35. The control circuit of claim 34, wherein

the flag signal has an inactive period and an active period,

the inactive period of the flag signal includes the active mode and the first refresh section of the stand-by mode, and

the active period of the flag signal includes the second refresh section.

36. The control circuit of claim 34, wherein

the detector circuit controls the oscillator circuit so that the period of the oscillation signal is lengthened after the first refresh section has elapsed, so that the period of the oscillation signal is the same in the active mode and in the first refresh section, and longer in the second refresh section.

37. The control circuit of claim 34, wherein the buffer circuit and detector circuit control the word line enable circuit so that a pulse width of the word line enable signal is wider in the first refresh section of the stand-by mode of operation than in the active mode.

38. The control circuit of claim 37, wherein the pulse width of the word line enable signal in the second refresh section is the same as in the first refresh section of the stand-by mode.

39. A method of controlling operation of a semiconductor memory device that includes an oscillation circuit and a word line enable circuit, the method comprising controlling the length of a period of the oscillation signal generated by the oscillation circuit and the pulse width of a word line enable signal generated by the word line enable circuit in response to the oscillation signal based on a change in mode of operation of the device.

40. A semiconductor memory device that is operated in accordance with the method of claim 27.

41. A semiconductor memory device, the operation of which is controlled in accordance with the method of claim 39.